What is claimed is:

1. A method for operating a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising the steps of:

(A) preparing a power-on mode for performing a DRAM operation; and

(B) preparing a power-off mode for holding stored data in the memory cell.

2. The method as recited in claim 1, wherein the step (A) includes the steps of:

(A-1) storing data hold in the floating gate into the capacitor; and

(A-2) adjusting a threshold voltage of the transistor in all of the memory cell to a first threshold voltage.

3. The method as recited in claim 1, wherein the step (B) includes the step of (B-1) moving the data stored in the capacitor to the floating gate.

4. The method as recited in claim 2, wherein the step (A-1) includes the steps of:

(A-1-a) charging the capacitors of all memory cell with a logic HIGH datum; and

(A-1-b) discharging the capacitor in the memory cell

having the transistor, its floating gate storing a logic high datum.

5. The method as recited in claim 4, wherein the step (A-1) includes the step of (A-1-c) refreshing the plurality of capacitors.

6. The method as recited in claim 5, wherein the plurality of the memory cells are arranged in a matrix by using a number of word lines and bit lines and the step (A-1) is carried out in a row-by-row basis.

7. The method as recited in claim 6, wherein the step (A-1-a) includes the steps of:

(A-1-a-1) supplying one word line connected to a multiplicity of the memory cells with a first threshold voltage in order to turn on the transistors in all of the memory cells;

(A-1-a-2) writing the logic HIGH datum in the capacitors of the memory cells coupled to the word line; and

(A-1-a-3) repeating the steps (A-1-a) and (A-1-b) until all of the capacitors in the plurality of the memory cells are charged with the logic HIGH datum.

8. The method as recited in claim 4, wherein the step (A-1-b) includes the steps of:

(A-1-b-1) supplying all of the word lines with a second

threshold voltage in order to turning on the transistors, its floating gate storing the logic HIGH datum; and

(A-1-b-2) supplying all of the bit lines with about 0 V in order to discharging the capacitors in the memory cell having the transistor, its floating gate storing the logic HIGH datum.

9. The method as recited in claim 1, wherein the step (A-2) includes the steps of:

(A-2-a) supplying all gates of the transistors in all of the memory cells with a first predetermined voltage in order for fulfilling electrons in the floating gate;

(A-2-b) charging all of the capacitors in all of the memory cells;

(A-2-c) decreasing the threshold voltage of the transistors to the first threshold voltage.

10. The method as recited in claim 9, wherein the step (A-2) including the steps of:

(E) backing up the captured data in the capacitor before the step (A-2-a); and

(F) restoring the backup data in the capacitor after the step (A-2-c).

11. The method as recited in claim 10, wherein the step (A-2-b) includes the steps of:

(A-2-b-1) supplying one side of the capacitor with about

0 V; and

(A-2-b-2) supplying the bit line with the logic HIGH datum.

12. The method as recited in claim 11, wherein the step (A-2-c) includes the steps of:

(A-2-c-1) removing electrons in the floating gate of the memory cells;

(A-2-c-2) discharging the capacitor by supplying gate of the transistor in the memory cells with the first threshold voltage; and

(A-2-c-3) repeating the steps (A-2-c-1) to (A-2-c-2) until all of the capacitors is discharged.

13. The method as recited in claim 12, wherein the step (A-2-c-1) includes the steps of:

(A-2-c-1-a) supplying a gate of the transistor in all of the memory cells with a negative voltage;

(A-2-c-1-b) supplying a plate of the capacitor in the memory cells with voltage level of a logic HIGH datum; and

(A-2-c-1-c) moving electrons in the floating gate to the capacitor storing the logic HIGH datum.

14. The method as recited in claim 13, wherein the step (A-2-c-2) includes the steps of:

(A-2-c-2-a) supplying the gate of the transistor with a second threshold voltage; and

(A-2-c-2-b) discharging the capacitor in some of the memory cells having the transistor turned on by the second threshold voltage.

15. The method as recited in claim 14, wherein the step (A-2) includes the step of (A-2-d) refreshing all of the memory cells.

16. The method as recited in claim 15, wherein the plurality of the memory cells are arranged in a matrix by using a number of word lines and bit lines and the step (A-2) is carried out in a row-by-row basis.

17. The method as recited in claim 13, wherein the capacitor is a coupling capacitor.

18. The method as recited in claim 3, wherein the step (B-1) includes the steps of:

(B-1-a) removing electrons in the floating gate of the memory cell storing a logic HIGH datum;

(B-1-b) discharging the capacitor by supplying gate of the transistor in all of the memory cells with a second threshold voltage; and

(B-1-c) repeating the steps (B-1-a) to (B-1-b) until all of the capacitors is discharged.

19. The method as recited in claim 18, wherein the step

(B-1-a) includes the steps of:

(B-1-a-1) supplying a gate of the transistor in all of the memory cells with a negative voltage;

(B-1-a-2) supplying a plate of the capacitor in the memory cells with voltage level of a logic HIGH datum; and

(B-1-a-3) selectively moving electrons in the floating gate to the capacitor storing the logic HIGH datum.

20. The method as recited in claim 18, wherein the step (B-1-b) includes the steps of:

(B-1-b-1) supplying the gate of the transistor with a second threshold voltage; and

(B-1-b-2) discharging the capacitor in some of the memory cells having the transistor turned on by the second threshold voltage.

21. The method as recited in claim 20, wherein the step (B-1-b) includes the steps of (B-1-b-c) refreshing the memory cell.

22. The method as recited in claim 21, wherein the step (B-1-b) is carried out row-by-row.

23. The method as recited in claim 19, wherein the capacitor is a coupling capacitor.

24. The method as recited in claim 2, wherein the step

(A-1) further includes the step of:

(A-1-a) supplying a word line with a voltage defined by the following equation:

$$V_{wl} = V_{blp} + (V_{th-H} + V_{th-L})/2$$

where V_{blp} is a bit line precharge voltage, V_{th-H} is a first threshold voltage, and V_{th-L} is a second threshold voltage; and

(A-1-b) writing logic HIGH or LOW data in the capacitor in response to whether the threshold voltage is the V_{th-H} or the V_{th-L}.

25. The method as recited in claim 23, wherein the step (A-1) includes the step of (A-1-c) refreshing the plurality of memory cells by supplying each word line with a voltage level being higher than the logic HIGH datum.

26. The method as recited in claim 25, wherein the step (A-1) is carried out row-by-row.

27. The method as recited in claim 26, wherein the step (A-1-a) further includes the step of (A-1-a-1) supplying other word lines with a predetermined negative voltage except for the word line supplied with the 'V_{wl}'.

28. A non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells in a matrix, wherein each memory cell includes:

a control gate layer coupled to a word line;

a capacitor for storing data;

a floating transistor for transmitting the stored data in the capacitor to a bit line; and

a first insulating layer between the control gate layer and the gate of the floating transistor,

wherein one side of the capacitor is coupled to a drain of the floating transistor and the other side of the same is supplied with a different voltage in response to the operation mode.

29. The NVDRAM device recited in claim 28, wherein the gate of the floating transistor is made of nitride.

30. The NVDRAM device recited in claim 29, wherein the gate of the floating transistor formed in a single layer serves as a data storage.

31. A non-volatile dynamic random access memory (NVDRAM) including a plurality of memory cells in a matrix, wherein each memory cell includes:

a control gate layer coupled to a word line;

a capacitor for storing data; and

a floating transistor for transmitting the stored data in the capacitor to a bit line,

wherein one side of the capacitor is coupled to a drain of the floating transistor and the other of the same is

supplied with each different voltage in response to the operation mode.

32. The NVDRAM device as recited in claim 31, wherein the control gate layer is made of metal and the gate of the floating transistor is made of nitride.

33. The NVDRAM recited in claim 32, wherein the gate of the floating transistor formed in a single layer serves as a data storage.